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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,934	03/06/2002	Amir Alon	IL920020007US1	7058

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IBM CORPORATION
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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,934	ALON ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-18 and 22-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,11-18 and 22-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/091,934 and Amendment filed on 01/23/2004. Claims 2-9, 11-18, 22-35 remain pending in the application. Claims 2-3, 5-6, 15-18 and 31-35 have been amended by changing term "critical interconnect line/wire" to "transmission line".

Based on the remarks and Amendment Examiner has performed additional search, and found new references.

2. The declaration submitted under 37 CFR 1.131 has been recorded. The declaration stales that prior to January 24, 20002, applicants had completed their invention. Applicants may have error stating that the invention had been reduced to practice prior to the filing date of Chang et al., January 24, 2001. The filing date of Chang should be January 24, 2002. However, since the effective date of Chang is July 9, 1999, Chang's patent application publication is still valid reference as 102 (e).

Claim Objections

3. Claims 22-28 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form.

4. Claim 31 is objected to because of the following informalities:

In claim 31, line 8 after "at least" insert – including--.

5. Claim 32 is objected to:

the recitation of "critical interconnect lines" and "transmission line topologies" are not clear to what applicants intend to mean. Additional information should be provided.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-7, 9 and 15-18 are rejected under 35 U.S.C. 102(b) as being unpatentable by Chao et al. (US Patent 5,031,111).

Chao discloses automated technique for the design of microwave and similar circuits using computer system including:

Independent claims:

(2) An integrated circuit design kit/system comprising (col.4, ll.40-67; col.5, ll.1-10; col.9, ll.34-59):

means/tools for generating one or more circuit component topologies (col.1, ll.5-10; col.2, ll.24-54; col.4, ll.15-39); and

means/tools for designing one or more transmission line topologies (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(6) A design topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(15) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored,

which when read by a computer, cause said computer to create a design topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8);

(17) A computer software circuit design product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream) said circuit design product, said circuit design product comprising means for designing topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8 and ll.26-54);

Dependent claims:

(3) The kit of claim 2 wherein said transmission line topologies are predefined (in a library) (col.5, ll.11-40);

(4) The kit of claim 2 further comprising one or more circuit component models (col.2, ll.24-67; col.3, ll.1-40);

(5) The kit of claim 2 and further comprising one or more transmission line models (col.2, ll.24-67; col.3, ll.1-40);

(7) The design topology of claim 6 wherein said topology is predefined (col.5, ll.11-40);

(9) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters (col.4, ll.15-39);

(16), (18) The product further comprising instructions, which when read by a computer, cause said computer lo create a design model of transmission lines (col.2, ll.24-67; col.3, ll.1-40);

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 2- 9 and 11-18 are rejected under 35 U.S.C. 102(e) as being unpatentable by Chang et al. (Pub. No.: US 2002/0104063).

Chang discloses method and system for extraction of parasitic interconnect impedance including inductance comprising:

Independent claims:

(2) An integrated circuit design kit/system comprising :

means/tools for generating one or more circuit component topologies ([0002]; [0003]; [0006]); and

means/tools for designing one or more transmission line (high speed/frequency interconnections) topologies (curves) ([0002]; [0003]; [0029]- [0032]);

(6) A design topology of transmission lines ([0003]; [0006]; [0029]-[0032]);

(15) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines ([0002]; [0003]; [0029]- [0032]);

(17) A computer software circuit design product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream) said circuit design product, said circuit design product comprising means for designing topology of transmission lines ([0002]; [0003]; [0029]- [0032]);

Dependent claims:

(3), (7) The kit wherein said transmission line topologies are predefined (interconnect primitive library) ([0011]; [0031]);

(4) The kit of claim 2 further comprising one or more circuit component models ([0012];[0013]);

(5) The kit of claim 2 and further comprising one or more transmission line models ([0028]);

(8) The topology of claim 6 comprising a definite current return path ([0043] and p.12, Claim2);

(9) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters ([0028];[0029]; [0032]; [0041]);

(11) The design topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires ([0080]-[0081]);

(12), (13), (14) The design topology, wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires ([0082]);

(16), (18) The product further comprising instructions, cause said computer lo create a design model of transmission lines ([0012]; [0013]).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Dangelo et al. (US Patent 5,555,201).

Dangelo teaches method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information comprising:

(30) A method for designing integrated circuits wherein defining a chip architecture and a floor plan comprises defining critical interconnect wires(col.16, ll.3-6, ll.13-16 and ll.35-47; col.17, ll.23-37 and ll.63-67; col.19, ll.65-67; col.20, ll.1-12; col.23, ll.66-67; col. 24, ll.1-2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 30 is rejected under 35 U.S.C. 102(e) as being unpatentable by Pileggi et al. (US Patent 6,367,051).

Pileggi recites method and system for concurrent buffer insertion and placement of logic gates including:

(30) A method for designing integrated circuits wherein defining a chip architecture and a floor plan comprises defining critical interconnect wires(col.1, ll.45-67; col.2, ll.1-26; col.3, ll.30-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 22-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (Pub. No.: US 2002/0104063) in view of Pileggi et al. (US Patent 6,367,051).

Independent claims:

Chang teaches method and system for extraction of parasitic interconnect impedance including:

(31) a system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more transmission lines models ([0002]; [0003]; [0006]; [0012];[0013]; [0028]); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more transmission line (high speed/frequency interconnections) topologies (curves) ([0002]; [0003]; [0016]; [0029]- [0032] ; [0034]-[0036]);

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(32) A method for designing integrated circuits (IC), said method comprising steps of:

b) identifying one or more critical interconnect lines/wire and defining one or more transmission line topologies for design of said critical interconnect lines ([0002]; [0003]; [0008]; [0029]- [0032]);

c) determining a schematic design (logic gate level circuit description) of said IC from said chip architecture, floor plan and said transmission line topologies ([0002]; [0003]; [0006]; [0029]- [0032]); and

d) defining a physical layout of said IC at least from said chip architecture, floor plan and said line topologies ([0002]; [0003]; [0016]; [0029]- [0032]; [0034]-[0036]).

With respect to claims 22-32 Chang teaches the features above but lacks a method for designing integrated circuits including defining a floor plan.

Pileggi recites system and method for concurrent buffer insertion and placement of logic gates, including:

A system for integrated circuit design comprising:

means/tools for designing a high level design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks and their locations are defined/mapping and further including one or more transmission line topologies (col.1, ll.45-67; col.2, ll.1-10 and ll.20-26 ; col.3,ll.30-61).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Pileegi's teaching regarding the method for designing integrated circuits (ICs) further comprising step of defining the floor plan and use it in Chang's invention to improve an efficiency of the IC design.

Dependent claims:

With respect to claims 23-33 Chang in view of Pileggi additionally describes:

(23), (29), (33) The method, wherein the step of designing comprises choosing from a set of predefined parameterized design topologies/cells ([0033]; [0034]);

(24) The method of claim 32, wherein in (b), the step of defining comprises

defining a set of design topologies ([0002]; [0003]; [0006]; [0029]- [0032]);

(25) The method according to claim 32, wherein said schematic design comprises models of said one or more transmission line topologies ([0012];[0013]);

(26) The method according to claim 25, and further comprising the step of calculating one or more electrical parameters of said models ([0002]; [0010]);

(27) The method according to claim 26, wherein said one or more electrical parameters includes one or more of the following: capacitance, low frequency inductance, high frequency inductance ([0028];[0029]; [0032]; [0041]);

(28) The method according to claim 32. wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, timing requirements ([0046]-[0048]).

With respect to claim 22 Pileggi in view of Chang additionally describes:

(22) The method of claim 32, wherein said integrated circuits are analog and mixed signal (AMS) circuits (col.2, ll.19-25; col.5, ll.28-42).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 34 and 35 are rejected under 35 U.S.C. 102(e) as being unpatentable by Chang et al. (Pub. No.: US 2002/0104063).

Chang discloses method and system for extraction of parasitic interconnect impedance including inductance comprising:

(34) A system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more transmission lines models, wherein said one or more transmission lines are models parameterized cells of one or more transmission lines topologies ([0002]; [0003]; [0006]; [0012];[0013]; [0028]; [0033]; [0034]);

(35) A method for designing integrated circuits (IC), said method comprising:

means/tools for designing a schematic design ([0002]; [0003]; [0006]; [0012];[0013]; [0028]); and

means/tools for designing a physical layout including at least one or more circuit components and one or more transmission line topologies, wherein said one or more transmission line topologies are parameterized cells of transmission lines ([0002]; [0003]; [0016]; [0029]- [0032]; [0033]-[0036]).

REMARKS

12. Examiner appreciates the detailed remarks offered by Applicant. However claims do not recite these specific particular limitations.

13. Mostly, the Applicant argues, "...the invention of the present application had been reduced to practice prior to the filing date of Chang et al., January 24, 2001." Filing date of Chang is January 24, 2002, but effective date of Chang is July 9, 1999 because this application is continuation of application No. 09/350,966, filed oh July 9, 1999, which is now US Patent 6,381,730 having filing date July 9, 1999. Therefore Chang is still valid reference as 102 (e).

14. Next the Applicant argues: " Dangelo et al. does not even begin to address or teach "designing one or more transmission line topologies", as cited in currently amended independent claims 2,6, 15, and 17, 31-35", and Applicant offers detailed remarks.

Examiner appreciates the detailed remarks offered by Applicant. However claims do not recite these specific particular limitations.

Applicant has amended claims 2-3, 5-6, 15-18 and 31-35 by changing term "critical interconnect line/wire" to "transmission line". Based on this amendment Examiner has found new references and rejected all pending claims under 35 U.S.C. 102(b), 102(e) and 103(a).

In view of the foregoing explanations, Examiner respectfully disagrees with Applicants that rejection of claims should be withdrawn.

15. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VUTHE SIEK
PRIMARY EXAMINER